

## IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1           1.       (Withdrawn) A baseband controller system, comprising:  
2           a plurality of buses coupled to communicate with a plurality of hardware blocks;  
3           a microsequencer also coupled to the plurality of buses;  
4           the microsequencer comprising a 72-bit correlator/ accumulator; and  
5           transceiver circuitry coupled to at least one of the plurality of buses.
- 1           2.       (Withdrawn) The baseband controller system of claim 1 wherein the  
2           microsequencer further comprises a 72-bit arithmetic logic unit.
- 1           3.       (Withdrawn) The baseband controller system of claim 1 wherein the  
2           microsequencer further comprises a plurality of temporary registers for storing computational  
3           data.
- 1           4.       (Withdrawn) The baseband controller system of claim 3 wherein the temporary  
2           registers include a 64-bit register.
- 1           5.       (Withdrawn) The baseband controller system of claim 3 wherein the temporary  
2           registers include a 48-bit register.
- 1           6.       (Withdrawn) The baseband controller system of claim 3 wherein the temporary  
2           registers include a 32-bit register.
- 1           7.       (Withdrawn) The baseband controller system of claim 3 wherein the temporary  
2           registers include a 16-bit register.
- 1           8.       (Withdrawn) The baseband controller system of claim 3 wherein the temporary  
2           registers include a 64-bit register, a 48-bit register, a 32-bit register and a 16-bit register.

1           9.       (Withdrawn) The baseband controller system of claim 8 further including logic  
2       circuitry to determine which temporary register should be used to store a piece of computational  
3       data based upon the size of the piece of computational data.

1           10.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of clocks, including a native Bluetooth clock.

1           11.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of clocks, including a native real-time clock.

1           12.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of clocks, including an externally driven Bluetooth clock.

1           13.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of clocks, including an externally driven real-time clock.

1           14.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of timers.

1           15.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer comprises a plurality of timers wherein the plurality of timers comprises at least  
3       four timers.

1           16.      (Withdrawn) The baseband controller system of claim 1 wherein the  
2       microsequencer includes eight timers.

1           17.      (Currently Amended) A microsequencer for use as a real-time Bluetooth baseband  
2       controller, ~~comprising~~ comprises:  
3               timer circuitry operably coupled to receive a requested timer counting value and to  
4       announce when the timer counting value has elapsed;  
5               temporary data storage circuitry operably coupled to store data; and

6 a plurality of Bluetooth and native clocks operably coupled to support ~~for supporting~~  
7 timing functionality of the timer circuitry according to Bluetooth specifications when in a master  
8 mode; and

9 a plurality of externally-driven Bluetooth and native clocks operably coupled to support  
10 timing functionality of the timer circuitry according to Bluetooth specifications when in a slave  
11 mode.

Claims 18 – 21 (Cancelled).

1 22. (Original) The microsequencer of claim 17 wherein the temporary data storage  
2 circuitry includes a 64-bit storage register.

1 23. (Original) The microsequencer of claim 17 wherein the temporary data storage  
2 circuitry includes a 48-bit storage register.

1 24. (Original) The microsequencer of claim 17 wherein the temporary data storage  
2 circuitry includes a 32-bit storage register.

1 25. (Original) The microsequencer of claim 17 wherein the temporary data storage  
2 circuitry includes a 16-bit storage register.

1 26. (Original) The microsequencer of claim 17 wherein the temporary data storage  
2 circuitry includes a 64-bit register, a 48-bit register, a 32-bit register and a 16-bit register.

1 27. (Currently Amended) The microsequencer of claim 17 wherein the temporary  
2 data storage circuitry ~~includes~~ comprises registers of different size and ~~further wherein the~~  
3 ~~microsequencer includes~~ a data storage logic module, which data storage logic module  
4 determines which available register should be used for storing the data based upon the size of the  
5 data that is to be temporarily stored.

1 28. (Currently Amended) The microsequencer of claim 17 wherein the ~~timers include~~  
2 timer circuitry comprises at least four timers.

1           29.     (Currently Amended) The ~~micro-sequencer~~ microsequencer of claim 17 wherein  
2 the ~~timers include~~ timer circuitry comprises at least eight timers.

1           30.     (Currently Amended) The ~~micro-sequencer~~ microsequencer of claim 27 further  
2 ~~including~~ comprises timer control logic circuitry for controlling the operation of the at least eight  
3 timers.

1           31.     (Original) A microsequencer for use as a real-time Bluetooth baseband controller,  
2 comprising:

3           eight timers to provide traditional timer functionality;  
4           timer control logic circuitry;  
5           an externally driven Bluetooth clock;  
6           an externally driven real-time clock;  
7           a native Bluetooth clock;  
8           a native real-time clock;  
9           a 64-bit register for temporarily storing computational data;  
10          a 48-bit storage register for temporarily storing computational data;  
11          a 32-bit storage register for temporarily storing computational data;  
12          a 16-bit storage register for temporarily storing computational data; and  
13          data storage logic circuitry for determining which of the temporary storage registers is to  
14 store a piece of data that is to be temporarily stored.

1           32.     (Original) The microsequencer of claim 31 wherein the period of one Bluetooth  
2 clock cycle is equal to 312.5 real-time clock cycle periods.